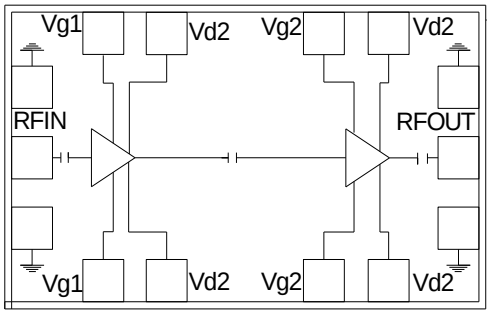
5 – 6 GHz 10 Watt Power Amplifier

Features

- **Frequency Range : 5 – 6GHz**
- **40.5 dBm Psat**
- **18 dB Power gain**
- **30% PAE**
- **High IP3**
- **Input Return Loss > 12 dB**
- **Output Return Loss > 7 dB**
- **Dual bias operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 5.3 x 5.5 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4006 is a C-band Power amplifier with 40dBm power output. The PA uses 2 stages of amplification and operates in 5 – 6 GHz frequency range. The PA features 18 dB of gain with input and output return losses of 12 dB and 7 dB respectively. The PA has a high IP3 of 47dBm and 30% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage.The die is fabricated using a reliable 0.5µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+9	volts
Drain current (Id)	4	A
RF input power (RFin at Vd=9V)	33	dBm
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.9V[4] Z_o =50 Ω, Pulse Duty Cycle = 10%

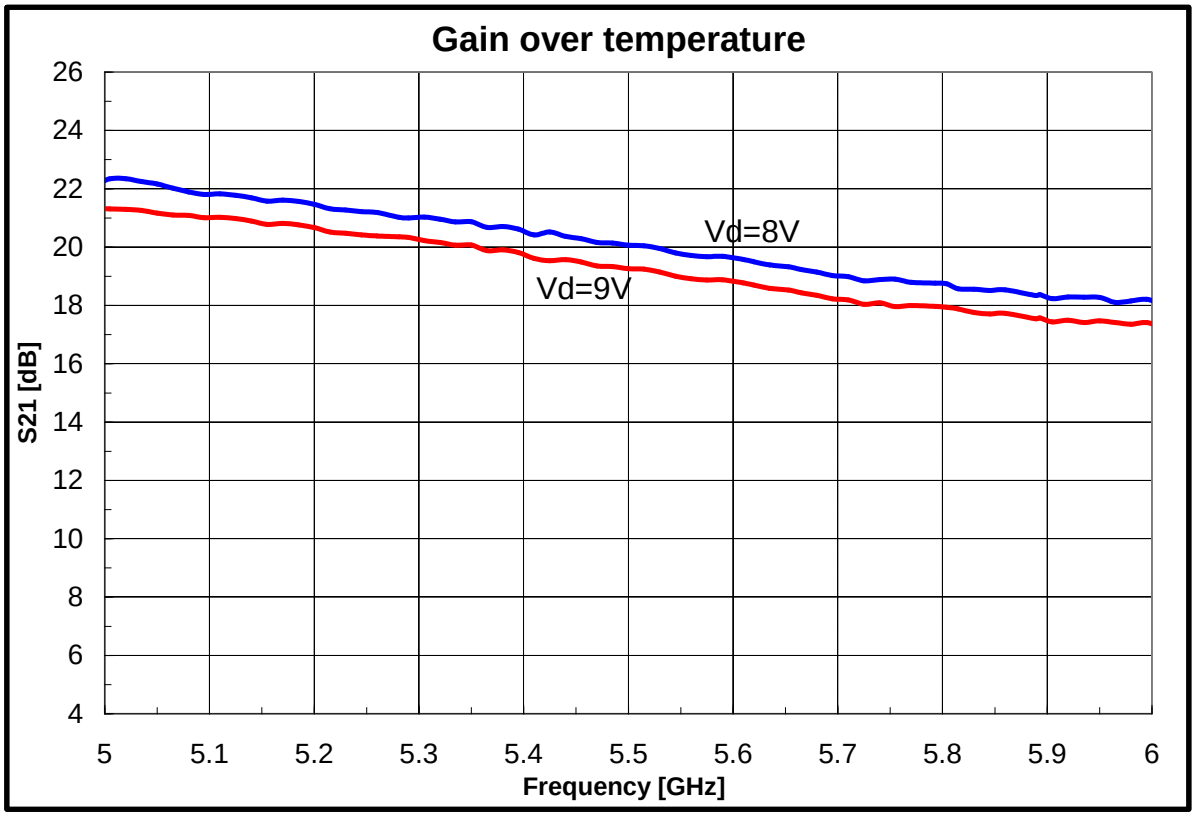
Parameter	Typ.	Units
Frequency Range	5 – 6	GHz
Gain	18	dB
Gain Flatness	+/-1.25	dB
Output Power (P1 dB)	39.5	dBm
Input Return Loss	12	dB
Output Return Loss	7	dB
Saturated output power (Psat)	40.5	dBm
Output Third Order Intercept (IP3)	47	dBm
Power Added Efficiency (PAE)[2]	30%	--
Supply Current(I_{dq})	2.9	A
Supply Current(I_{dsat})[3]	3.4	A

Note:

1. Electrical specifications as measured in test fixture.
2. PAE measured at 2dB Gain Compression Point.
3. I_{dsat} is the maximum drain current under input RF drive.
4. Gate voltage "V_g" of the PA need to be adjusted with in the range of (-0.7V to -1.2V) in order to set the required value of quiescent drain current "I_{dq}".

Test fixture data

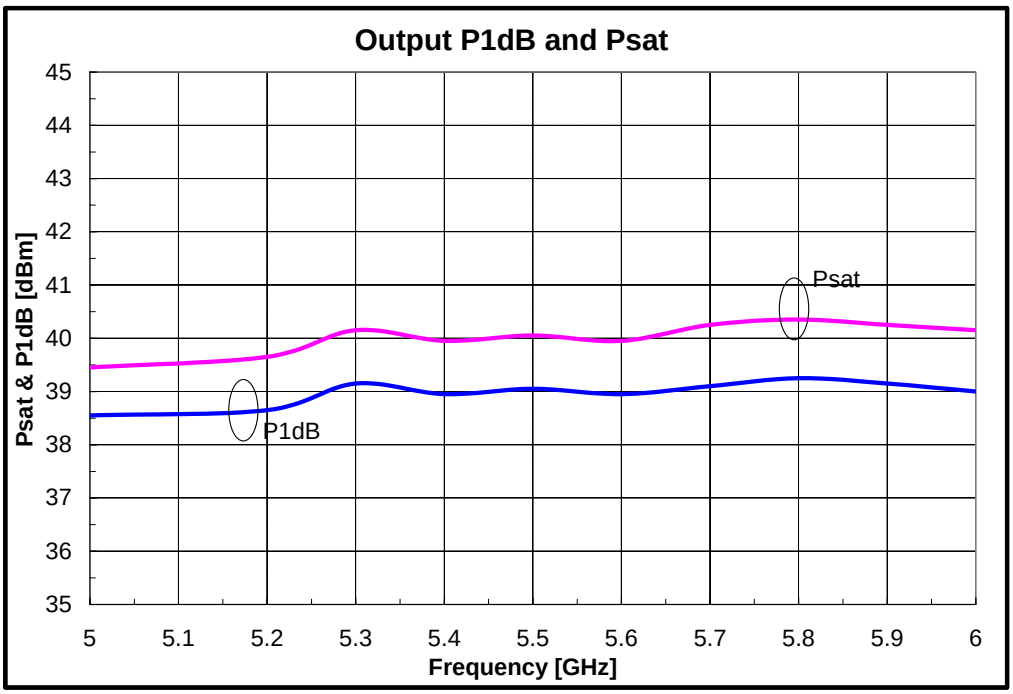
V_{d1} = V_{d2} = Vd, V_{g1} = V_{g2} = -0.9V, Total Current =2.9A, T_A = 25 °C, Pulse Duty Cycle = 10%



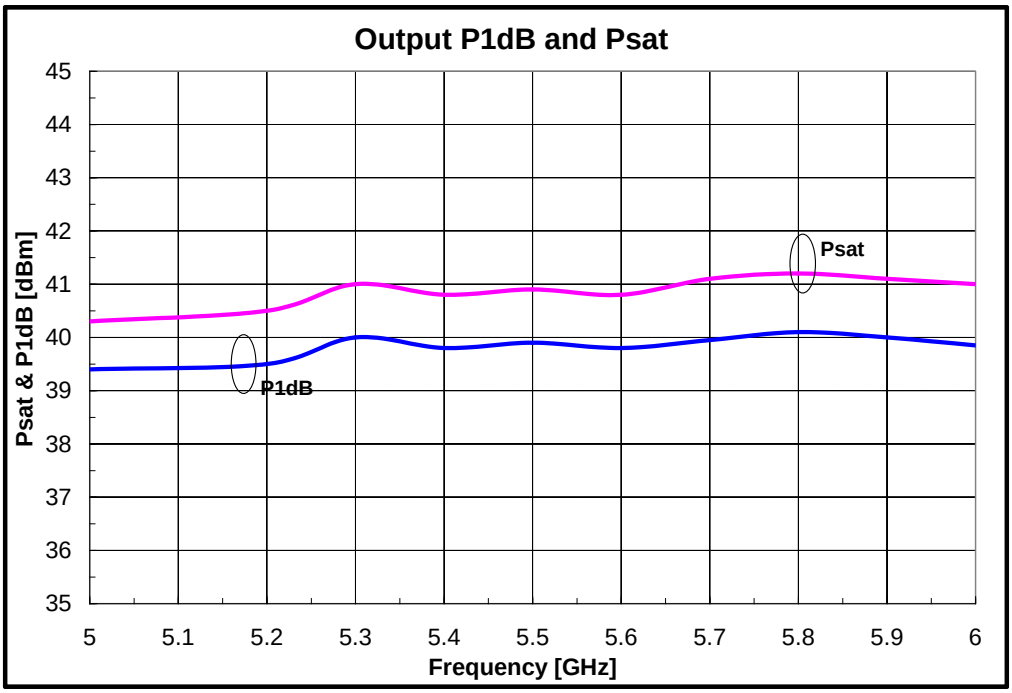
Gain at Vd = 8V and Vd = 9V bias

Test fixture data

V_{d1} = V_{d2} = Vd, V_{g1} = V_{g2} = -0.9V, Total Current =2.9A, T_A = 25 °C, Pulse Duty Cycle = 10%



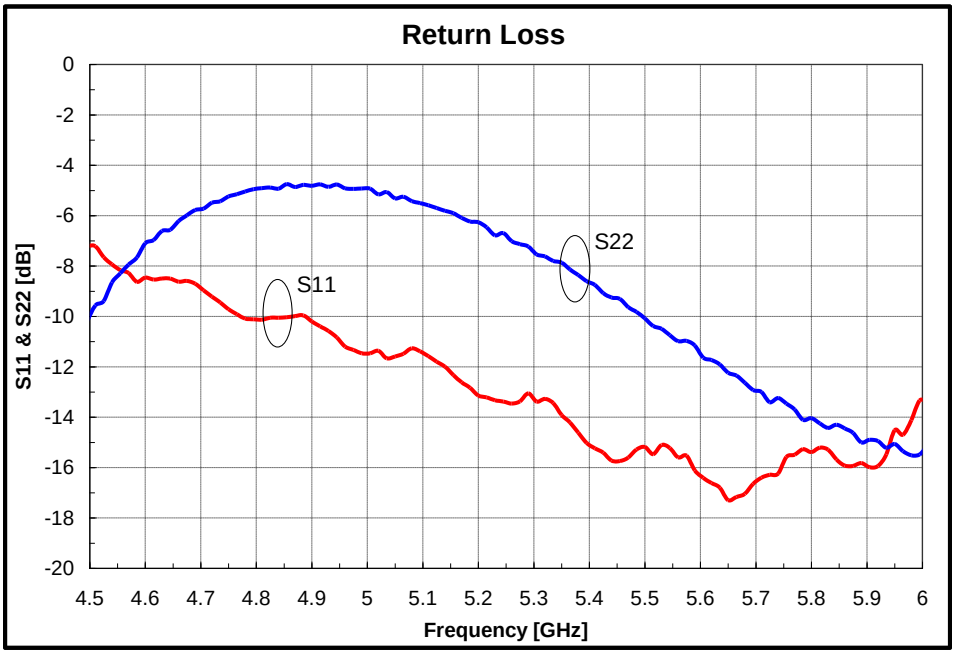
Output Power at Vd = 8V

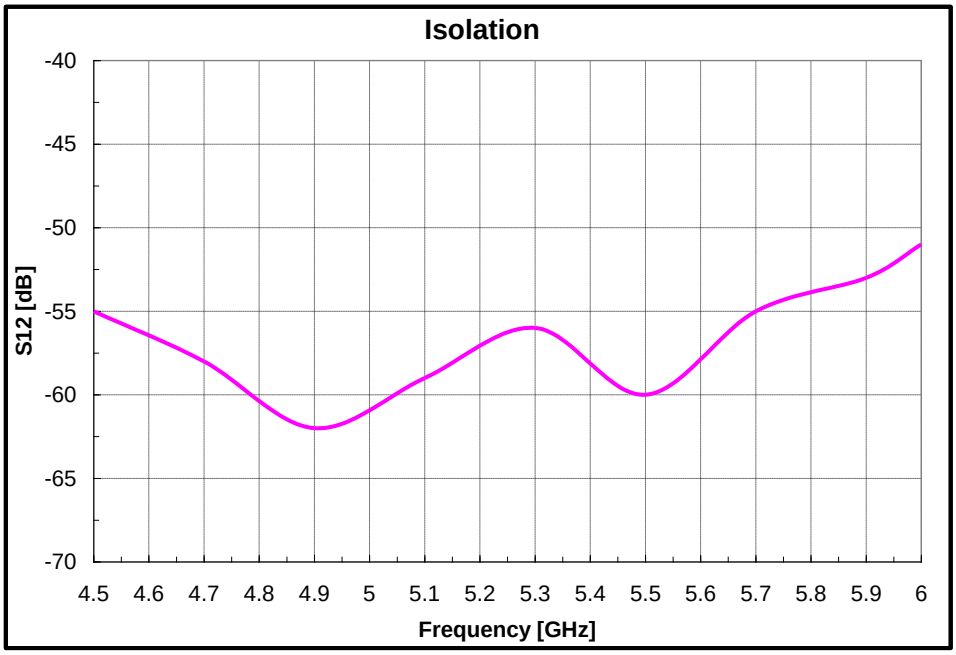


Output Power at Vd = 9V

Test fixture data

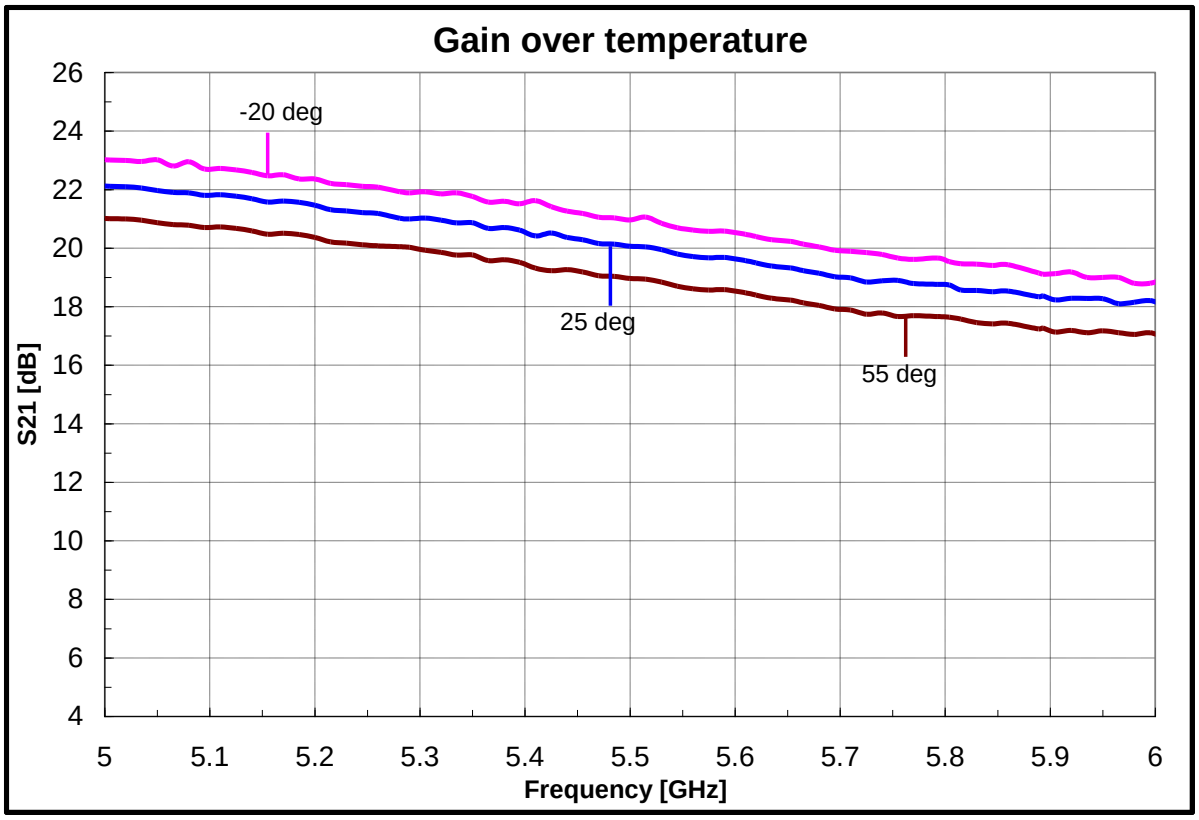
V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.9V, Total Current =2.9A, T_A = 25 °C, Pulse Duty Cycle = 10%





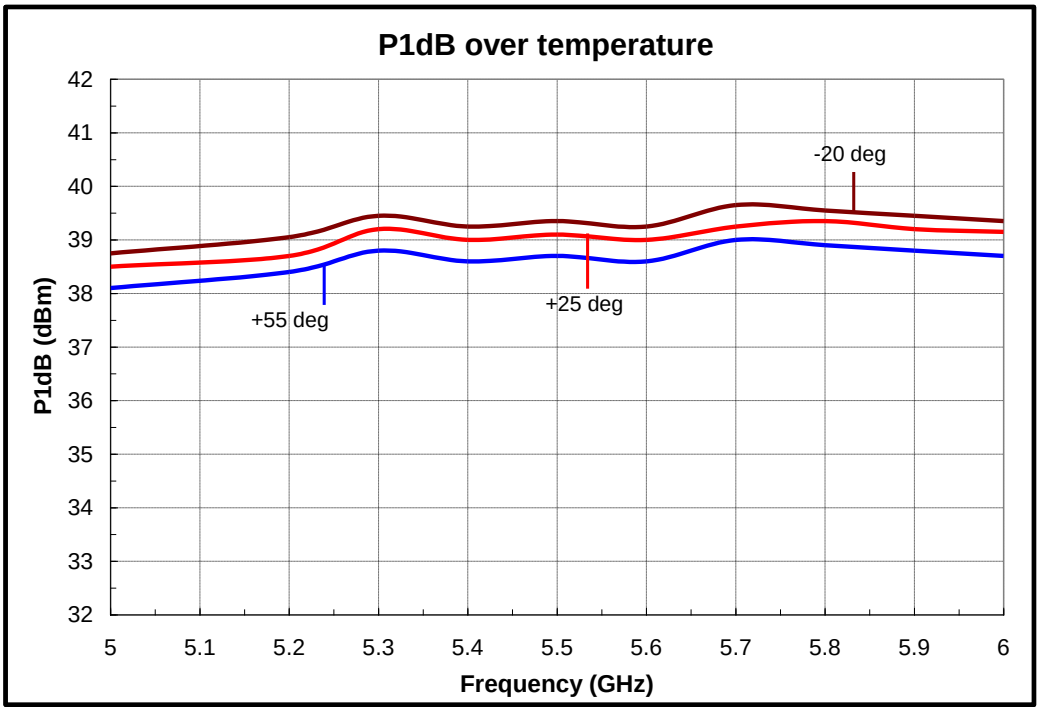
Temperature data

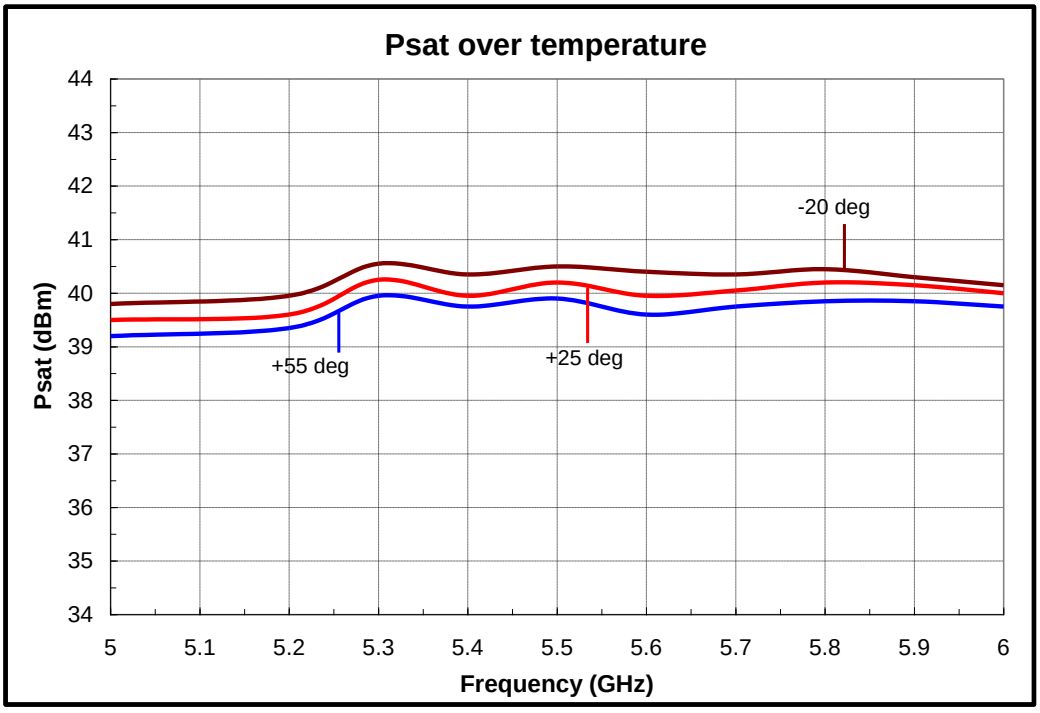
V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.9V, Total Current =2.9A, T_A = 25 °C, Pulse Duty Cycle = 10%



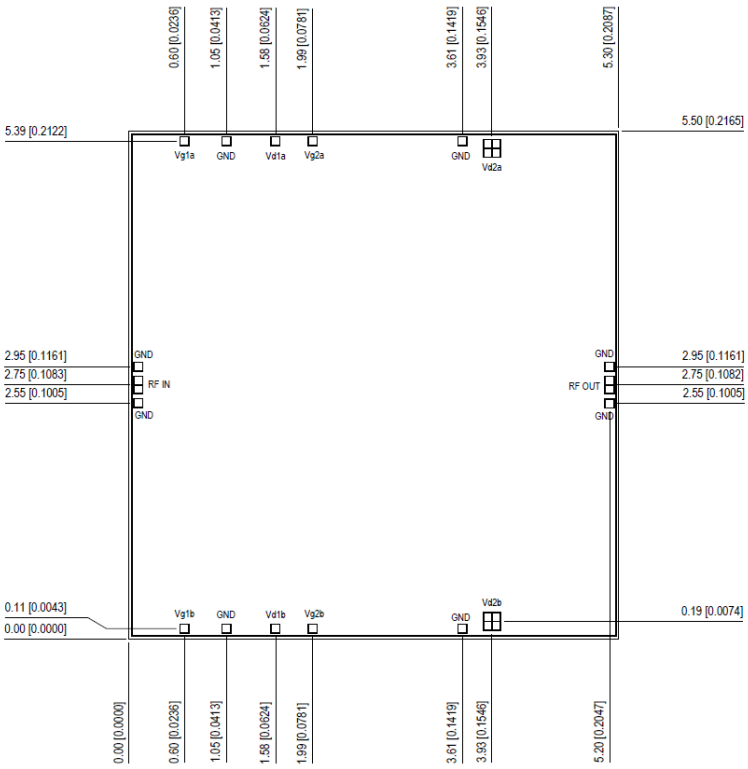
Temperature data

V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.9V, Total Current =2.9A, T_A = 25 °C, Pulse Duty Cycle = 10%





Bond Pad Locations

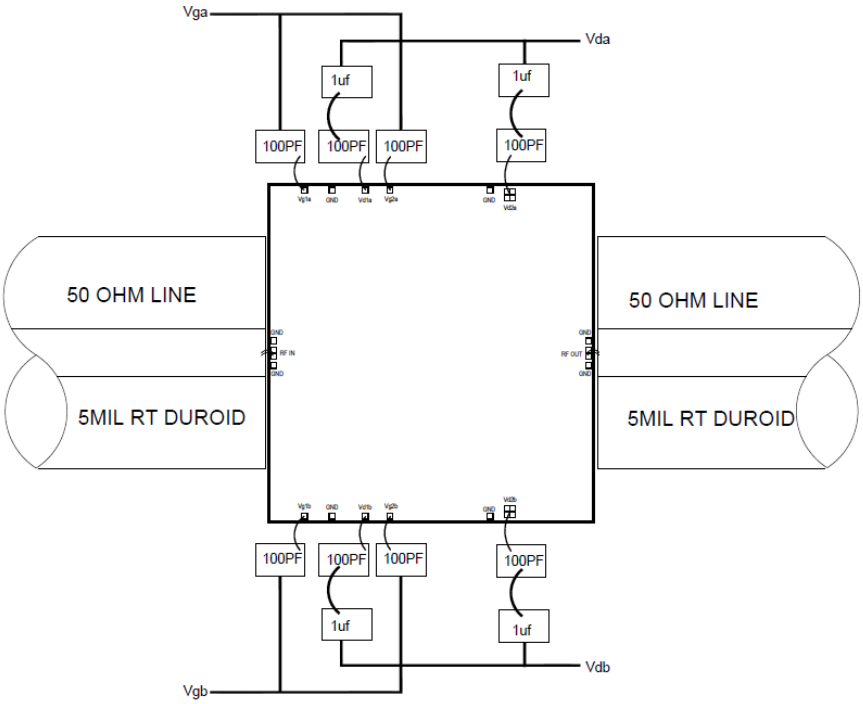


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Bond Pad "RFIN" : RF Input
3. Bond Pad "Vg1a" : 1st stage gate voltage(V_{g1}) towards north
4. Bond Pad "Vg1b" : 1st stage gate voltage(V_{g1}) towards south
5. Bond Pad "Vd1a" : 1st stage drain voltage(V_{d1}) towards north
6. Bond Pad "Vd1b" : 1st stage drain voltage(V_{d1}) towards south
7. Bond Pad "Vg2a" : 2nd stage gate voltage(V_{g2}) towards north
8. Bond Pad "Vg2b" : 2nd stage gate voltage(V_{g2}) towards south
9. Bond Pad "Vd2a" : 2nd stage drain voltage(V_{d2}) towards north
10. Bond Pad "Vd2b" : 2nd stage drain voltage(V_{d2}) towards south
11. Bond Pad "RFOUT" : RF Output

Recommended Assembly Diagram



Note :

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF Single Layer Bypass Capacitor.
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate
4. 1µF capacitors may be additionally used as a second level of bypass.
5. The RF input & output ports are DC decoupled on-chip.
6. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip

Die attach: Eutectic attachment using flux less AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 to 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice. Before using the product, please refer to the latest datasheet available in the website.